CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A processing machine comprising:

(a) a data memory;

(b) a control engine, linked in communication with the data memory;

(c) an instruction memory in which instructions may be stored, having an input for receiving control information from the control engine; and

(d) a plurality of coprocessors, each connected in communication with the data memory, the instruction memory, and the control engine, the control engine and the plurality of coprocessors coupled to receive a single instruction from the instruction memory in parallel, each of said control engine and plurality of coprocessors being enabled to perform simultaneous functions in response to [[a]]the single instruction.

2. (Original) The processing machine of claim 1, wherein the control engine comprises a microcontroller.

3. (Original) The processing machine of claim 1, further comprising a main memory linked in communication with at least one of said plurality of coprocessors.

4. (Original) The processing machine of claim 3, wherein said at least one coprocessor comprises a bus interface coprocessor.

5. (Original) The processing machine of claim 1, wherein the processing machine is used to perform a particular task and wherein each coprocessor is designated to perform at least one specific subtask of that particular task.

6. (Original) The processing machine of claim 5, wherein the particular task comprises processing a data manipulation algorithm, and specific subtasks performed by separate coprocessors include a memory bus interface function and a data processing algorithm function.

7. (Original) The processing machine of claim 6, wherein the data processing algorithm comprises an encryption algorithm.

8. (Currently Amended) A processing machine comprising:

(a) a data memory;

(b) a main memory;

(c) a microcontroller, linked in communication with the data memory;

(d) an instruction memory in which instructions may be stored, having an input for receiving control information from the microcontroller, the microcontroller having an input to receive instructions from the instruction memory;

(e) a first coprocessor providing a bus interface function when operational, linked in communication with each of the main memory, the data memory, and the microcontroller, and having an input to receive instructions from the instruction memory; and

(f) a second coprocessor, linked in communication with the data memory and the microcontroller and having an input to receive instructions from the instruction memory, wherein ~~the data memory,~~ the microcontroller~~, the instruction memory,~~ and the first and second coprocessors are coupled to receive the instructions from the instruction memory in parallel.

9. (Original) The processing machine of claim 8, further comprising:

a third coprocessor, linked in communication with the data memory and the microcontroller and having an input to receive instructions from the instruction memory.

10. (Original) The processing machine of claim 9, further comprising:

a fourth coprocessor, linked in communication with the data memory and the microcontroller and having an input to receive instructions from the instruction memory.

11. (Previously Presented) The processing machine of claim 8, wherein each of the first and second coprocessors and the microcontroller perform simultaneous coordinated functions in response to a single instruction issued from the instruction memory.

12. (Original) The processing machine of claim 8, wherein the second coprocessor is enabled to process a data manipulation algorithm.

13. (Previously Presented) The processing machine of claim 9, wherein the third coprocessor is enabled to perform an ATM data transfer interface function.

14. (Previously Presented) The processing machine of claim 10, wherein the third coprocessor is enabled to perform an ATM data transfer interface function when operational and the fourth coprocessor is enabled to perform an ATM Adaptation Layer (AAL) function when operational.

15. (Currently Amended) A method of processing a data manipulation task with a processing machine including a control engine and a plurality of coprocessors~~ coupled in parallel~~, comprising;

dividing the data manipulation task into a plurality of subtasks;

issuing a sequence of instructions having a plurality of portions to the control engine and each of said plurality of coprocessors;

simultaneously receiving corresponding portions of the instructions in parallel at the control engine and each of said plurality of coprocessors;

performing separate subtasks with the control engine and each of said plurality of coprocessors~~ in response to~~ by executing the corresponding portions of the instructions received by~~ each of these components~~ the control engine and each of said plurality of coprocessors; and

coordinating [[an]]the execution of each portion of instructions received by the control engine and each of said plurality of coprocessors such that the subtasks performed by these components are performed substantially in parallel.

16. (Original) The method of claim 15, wherein the coordination of the execution of the portions of instructions is performed by the control engine via execution control signals sent to each of said plurality of coprocessors.

17. (Original) The method of claim 16, wherein the processing machine comprises a programmed state machine and wherein each of the control engine and said plurality of coprocessors is caused to cycle through a respective set of machine states in response to instruction portions received by that component.

18. (Original) The method of claim 15, wherein one of the subtasks comprises a bus interface function.

19. (Original) The method of claim 15, wherein the control engine comprises a microcontroller.

20. (Original) The method of claim 15, wherein each instruction is issued from an instruction memory in response to an address sent to the instruction memory from the control engine.